IN THE CLAIMS

Please cancel claim 1 without prejudice or disclaimer.

Applicants note that claim 2 is not amended to overcome prior art but to be written in independent form. Further, Applicants note that claims 3 and 4 are not amended to overcome prior art but to provide consistency with the cancellation of claim 1. Further, Applicants note that claim 4 is not amended to overcome prior art but to correct a typographical error. The amendments made to claims 2-4 are not narrowing in scope and therefore no prosecution history estoppel arises from the amendments to claims 2-4. *Festo Corp v. Shoketsu Kinzoku Kogyo Kabushiki Co.*, 62 USPQ2d 1705, 1711-1712 (2002); 56 USPQ2d 1865, 1870 (Fed. Cir. 2000). Further, the amendments made to claims 2-4 were not made for a substantial reason related to patentability and therefore no prosecution history estoppel arises from such amendments. *See Festo Corp.*, 62 USPQ2d 1705 at 1707 (2002); *Warner-Jenkinson Co. v. Hilton Davis Chemical Co.*, 41 USPQ2d 1865, 1873 (U.S. 1997).

Claim 1 (canceled)

Claim 2 (currently amended): [The semiconductor device of claim 1] A semiconductor device including a core and a periphery, the semiconductor device comprising:

a plurality of core gate stacks in the core, each of the plurality of core gate stacks including a first polysilicon gate and a WSi layer above the first polysilicon gate, wherein each of the plurality of core gate stacks includes an edge[, the semiconductor device further comprising:];

a plurality of core spacers, each of the plurality of core spacers residing along an edge of the plurality core gate stacks;

a plurality of sources in the core, the plurality of sources residing between a portion of the plurality of core gate stacks; and

a plurality of periphery gate stacks in the periphery, each of the plurality of periphery gate stacks including a second polysilicon gate and a CoSi layer on the second polysilicon gate.

Claim 3 (currently amended): The semiconductor device of claim [1] 2 wherein each of the plurality of periphery gate stacks includes an edge, the semiconductor device further comprising:

a plurality of periphery spacers, each of the plurality of periphery spacers residing along an edge of the plurality periphery gate stacks.

Claim 4 (currently amended): The semiconductor device of claim [1] 2 wherein each of the plurality of core gate stacks includes the first polysilicon gate, the WSi layer above the first polysilicon gate, a layer of polysilicon above the WSi layer and a capping layer above the [WSi layer] layer of polysilicon.

Claim 5 (original): The semiconductor device of claim 4 wherein the capping layer is a SiN layer.

Claim 6 (original): The semiconductor device of claim 4 wherein the capping layer is a SiON layer.

Claims 7-15 (withdrawn)

Claim 16 (new): A semiconductor device comprising:

a plurality of core gate stacks in a core, wherein each of said plurality of core gate stacks comprises a first polysilicon gate and a WSi layer above said first polysilicon gate and a polysilicon capping layer above said WSi layer and an additional capping layer above said polysilicon capping layer;

a plurality of sources in said core, wherein said plurality of sources resides between a portion of said plurality of core gate stacks; and

a plurality of periphery gate stacks in a periphery, wherein each of said plurality of periphery gate stacks comprises a second polysilicon gate and a CoSi layer above said second polysilicon gate.

Claim 17 (new): The semiconductor device as recited in claim 16, wherein said additional capping layer functions as an antireflective layer.

Claim 18 (new): The semiconductor device as recited in claim 16, wherein said additional capping layer is a SiN layer.

Claim 19 (new): The semiconductor device as recited in claim 16, wherein said additional capping layer is a SiON layer.